

FLOATING POINT DIVIDER WITH EMBEDDED STATUS INFORMATION

Abstract of the Disclosure

A system for providing a floating point division comprises an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively. In addition, the system comprises a results circuit coupled to the analyzer circuit. The results circuit is configured to assert a resulting floating point operand containing the result of the division of the first floating point operand by the second floating point operand. Additionally, the results circuit provides resulting status embedded within the resulting floating point operand.